LISTING OF THE CLAIMS

The following claims are amended as follows:

1. (Currently amended) A ~~process~~ method for outputting a digital signal, the ~~process~~ method comprising the steps of:

supplying a driver stage with a current via a positive and a negative current supply connection;

limiting the current to a current limit value via a positive and/or negative current supply connection; and

temporarily increasing the current flowing via an output of the driver stage in synchronization with the edges of at least one trigger signal of the driver stage, wherein the increased current is provided via a capacitor to increase the output current of the driver stage.

2. (Currently amended) The ~~process~~ method according the Claim 1, further comprising a step of the driver stage supplying a differential output signal at two output lines wherein at least one of the two output lines receives the increase signal.

3. (Currently amended) The ~~process~~ method according to Claim 1, wherein the step of providing an increase signal comprises providing an increase signal generated with a time delay to the corresponding edge of the at least one trigger signal of the driver stage.

4. (Currently amended) The ~~process~~ method according to Claim 3, wherein the step of providing an increase signal comprises providing an increase signal generated by an inverting or a non-inverting driver which receives a control signal at its input.

5. (Currently amended) The ~~process~~ method according to Claim 1, wherein the step of increasing the current comprises increasing the current via a capacitor having a variable capacitance.

6. (Currently amended) The ~~process~~ method according to Claim 1, wherein the step of increasing the current via a capacitor comprises providing a current having a voltage increase which is greater than the voltage increase of the output signal of the driver stage.

7. (Currently amended) The ~~process~~ method according to Claim 1, wherein the step of supplying a driver stage with a current comprises providing a constant current.

8. (Currently amended) The ~~process~~ method according to Claim 1, further comprising a step of the driver stage supplying a differential output signal at two output lines wherein the current flowing via the positive supply connection and the current flowing via the negative current supply connection are controlled such that the mean value of the voltages of the two output lines assumes a controlled constant value.

9. (Currently amended) The ~~process~~ method according to Claim 1, wherein the step of supplying the driver stage with a current comprises supplying the driver stage with current from a controllable current source via the positive and/or negative current supply connection and at least one controllable current source receives an increased current via a capacitor.

10. (Currently amended) The ~~process~~ method according to Claim 9, wherein the output of the capacitor is terminated with a terminal resistor and the capacitance of the capacitor together with the terminal resistance forms a time function element, the time constant of which is less than the minimum period occurring in the digital signal to be output between two successive edges of a control signal.

11. (Original) A device for outputting a digital signal, the device comprising:

a driver stage receiving a supply current via a positive and a negative current supply connection, wherein the current via the positive and/or negative current supply connection is limited to a current limit value;

a current increase signal increasing the current flowing via an output of the driver stage in synchronization with the edges of at least one control signal of the driver stage; and

a capacitor generating an increased current to increase the output current of the driver stage.

12. (Original) The device according to claim 11, wherein the driver stage is designed such that it supplies a differential output signal at two input lines;

wherein the two output lines are connected to a capacitor to receive the increased current via the capacitor.

13. (Original) The device according to claim 11, wherein the device generates at least one current increase signal with a time delay to the corresponding edge of the at least one trigger signal of the driver stage.

14. (Original) The device according to claim 13, wherein the device comprises an inverting driver and a non-inverting driver which receives a control signal at its input for generating the at least one increase signal.

15. (Original) The device according to Claim 11, wherein the at least one capacitor has a variable capacitance.

16. (Original) The device according to Claim 11, wherein the voltage increase of the increase signal is greater than the voltage increase of the output signal of the driver stage.

17. (Original) The device according to claim 11, further comprising controlling means for controlling the current flowing via the positive and/or negative current supply connection to a constant value.

18. (Original) The device according to Claim 11, wherein the driver stage supplies a differential output signal at two output lines and wherein the device further comprises controlling means for controlling the current flowing via the positive supply connection and the current flowing via the negative current supply connection such that the mean value of the voltages of the two output lines assumes a controlled constant value.

19. (Currently amended) The device according to Claim 11, wherein the device ~~comprising~~ further comprises a controllable current source for supplying the driver stage with current via the positive and/or negative current supply connection and at least one controllable current source which is connected to a capacitor to receive the current increase signal therefrom.

20. (Original) The device according to Claim 19, wherein the output of the capacitor is terminated with a terminal resistor and the capacitance of the capacitor together with the terminal resistance forms a time function element, the time constant of which is less than the minimum period occurring in the digital signal to be output between two successive edges of a control signal.